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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/523,087	02/02/2005	Wilhelm Melchert	20798/0204621-US0	8536

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EXAMINER	
KITOV, ZEEV V	

ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,087	MELCHERT ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7 - 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on May 21, 2007. Claims and 15 - 17 are amended. Amendment has overcome rejection under USC 112, 1st paragraph. A new Office action follows.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 8, 10, 12 - 14, 16, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Lempo et al. (EP 0 091 648) in view of Maier et al. (FR 2,808,619) and Seiler et al. (US 4,178,619). Regarding Claim 7, Van Lempo et al. disclose following elements: a timer (R1 – R3, C and T1 in Fig. 4), a first switching device (voltage follower) (T5 in Fig. 4) including a first output (upper terminal of the coil) connected in series with an operating coil (L in Fig. 4), the first switching device is active for a duration of a pickup phase after the control voltage has been applied via the timer; a second switching device (T3 in Fig. 4) connected in series with the operating coil (L in Fig. 4), the second switching device being turned on as long as the control voltage (U3 in Fig. 4) is present. It further discloses the voltage source (U1 in Fig. 4) configured to

activate the first switching device (T5 in Fig. 4) by a pickup voltage (short duration pulse); the voltage is controlled by the timer (R1 – R3, C, T1 in Fig. 4).

The operating coil and the switching path of the second switching device form a series circuit connected to the first output (upper terminal of the coil); the series circuit and the first switching device are suppliable with the operating voltage (by the power supply U1 in fig. 4).

However, it does not disclose the rectifier circuit. Maier et al. disclose the rectifier circuit (4 in Fig. 1) connected to the control input (2 – 3 in Fig. 1) providing a second output (Uv in Fig. 1) and inherently supplying smoothed operational voltage, since otherwise the voltage regulator (8 in Fig. 1) would be unable to supply a steady DC voltage. It further discloses the step-down voltage converter (5 in Fig. 1) providing a step-down voltage at the third output supplying voltage to microprocessor (timer) 6 in Fig. 1. The reference has the same problem solving area, namely providing schematic for driving the solenoids. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Van Lempo et al. solution by adding the rectifier and voltage reducing circuit according to teachings of Maier et al., because (a) as Maier states ([0003]), the coil driving circuit is to be used in the power distribution networks "bang – bang" controllers, which as well known in the art, operate with the AC input signals, which are to be rectified in order to be processed by the microprocessor, such as element 6 in Fig. 1, and (b) the step-down voltage converter is to be used to convert the high value AC voltage typical for the power distribution networks to the low voltage value suitable for a power supply of the microprocessor.

In the Van Lempo et al. system modified according to teachings of Maier et al. the timer is activated by application (ramping) of the operating voltage. As to a connection between the outputs and the input, Maier et al. disclose the step-down voltage converter (5 in Fig. 1) providing a step-down voltage at the third output supplying the low voltage to feed microprocessor (timer) 6, the equivalent to Van Lempo et al. system is a low voltage power supply U2 in Fig. 4. It additionally discloses the voltage stabilizer (8 in Fig. 1), which inherently performs stepping down a voltage in stabilization process, the voltage stabilizer provides a power supply to the solenoid (7 in Fig. 1); the voltage stabilizer output may also be considered as the third output.

As to a forward biased diode, the diode D2 in the Van Lempo et al. circuit addresses this limitation by providing connection between the low voltage power supply U2 (which is analog to the voltage converter 5 in Maier et al. circuit) and the first output (at the emitter of transistor T5 in Van Lempo et al.); the isolation diode (D2 in Fig. 4) is forward biased whenever the second switch (T1 in Fig. 4) is ON. Therefore, in the Van Lempo et al. circuit modified according to teachings of Maier, the first and the third outputs are interconnected via forward biased diode.

However, it does not disclose the connection of the first output to the control input of the second switch. Seiler et al. disclose the switch (28 in Fig. 4 and 5) similar to the second switch of Van Lempo et al., i.e. positioned between the solenoid and the ground terminal, and including the protecting diode (23 in Fig. 3 – 5) connecting the first terminal (the upper terminal of the switch) with the control input of the second switch. The reference has the same problem solving area, namely driving the inductive loads by

semiconductor switching devices. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Van Lempo et al., solution by adding the protecting diode connected between the upper terminal of the second switching device and its control input, because as Seiler et al. state (col. 1, lines 10 – 44), the semiconductor switching devices used for switching of the inductive load are to be protected against over-voltages.

Regarding Claim 8, Van Lempo et al. disclose the electromagnetic switching device used for switching of magnetic valves, which inherently include the operating mechanism.

Regarding Claim 10, Van Lempo et al. disclose the differentiating RC element (R2 – R3, C in Fig. 4), providing the output voltage taken across the resistive element (R3 in Fig. 4).

Regarding Claim 12, Van Lempo et al. disclose the RC element combined with a voltage-limiting device (diode D4 in Fig. 4).

Regarding Claims 14 and 19, Seiler et al. disclose a free - wheeling device (111 and 17, 18 in Fig. 2) connected in parallel with the switching path of the second switching device (11 in Fig. 2). A motivation for modification of the primary reference is the same as above.

Regarding Claims 13 and 16, Van Lempo et al. disclose the voltage source (U1 in Fig. 4), which being controlled by the timer (R1 – R3, C in Fig. 4) includes a voltage limiting circuit (D4 in Fig. 4) and a threshold element (base-emitter junction of transistor T4 in Fig. 4); the voltage limiting circuit being supplied with the operating voltage (U1 in

Fig. 4) and having a fourth output connected to a switching path of a threshold circuit (base of T4 in Fig. 4), the threshold circuit being connected to the timer on an output side thereof.

Claims 9, 11, 15, 17, 18 and 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Lempo et al. in view of Maier et al., Seiler et al. and Saunders (US 4,633,362). As per Claim 9, it differs from Claim 7 rejected above by its limitation of including an integrating RC element. Van Lempo et al. disclose the pulse shaping circuit including a differentiating RC element (R1 – R3, C in Fig. 4). Saunders discloses the solenoid driving circuit (Fig. 5) wherein the circuit determining the solenoid driving pulse duration is a monostable circuit built around "555/556 timer" (the name universally used in the industry, U3b in Fig. 5) having the integrating RC circuit (R19, C6 in Fig. 5), which sets the duration of pulse. The reference has the same problem solving area, namely setting the solenoid driving pulse duration. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Van Lempo et al. solution by changing the differentiating RC circuit to the integrating RC circuit according to teachings of Saunders, because in modern electronic design use of integrated circuit timers, such as famous 555/556-type shown by Saunders, is universally excepted; an obvious advantage of such solution is the same as advantages of integration circuits vs. separate parts solutions, i.e. reliability, lower cost in assembly, easier troubleshooting. Additionally, the integrating RC circuit providers an advantage vs. the differentiating RC circuit in its higher noise immunity.

Regarding Claim 11, the 555/556-type timer used by Saunders inherently has its voltage-limiting device; i.e. according to Berlin textbook "The 555 timer Applications" (Fig. 2-2, pages 15 – 18), when the capacitor voltage reaches value 2/3 of the power supply voltage, the discharge transistor Q1 is activated (pin 13, DIS in Fig. 5 of Saunders, corresponding to pin 7 in Fig. 2-2 of Berlin) and discharges the capacitor thus preventing the capacitor from obtaining excessive value voltage. Pin numbers of the 555 and 556 versions of the same timer are disclosed by Berlin in Fig. 1-1B and 1-2. A motivation for modification of the primary reference is the same as above.

Regarding Claims 15 and 17, in the Van Lempo et al. circuit modified according to teachings of Saunders, i.e. having the RC circuit solution replaced by the 555/556 timer of Saunders, all the elements of Claim 15 are present; as was stated above (see Claim 11 rejection) the voltage limiting circuit is inherently present in the 555/556 timer; the threshold circuit with comparator are inherent in the structure of 555 timer (see upper comparator connected to pin 6 in 555 version in the Figure 2-2 of Berlin). A motivation for modification of the primary reference is the same as above.

Regarding Claim 17, in the Van Lempo et al. circuit modified according to teachings of Saunders, the voltage limiting circuit (transistor connected to output 7 in Figure 2-2 of Berlin) inherently being supplied with the operating voltage and has fourth output (pin 7 in Figure), which is connected to a switching path of a threshold circuit, i.e. to a threshold pin 6 in Figure 2-2 of Berlin), the threshold circuit being connected to the switching (discharge) path of a threshold circuit, i.e. middle junction of the time constant circuit RC (output of RC).

Regarding Claims 18 and 20, Seiler et al. disclose a free - wheeling device (111 and 17, 18 in Fig. 2) connected in parallel with the switching path of the second switching device (11 in Fig. 2). A motivation for modification of the primary reference is the same as above.

Response to Arguments

Applicant's arguments have been fully considered but they are not persuasive.

Applicant attacks the Seiler et al. reference for allegedly not disclosing a forward biased diode. However, the Seiler et al. reference is not intended to disclose that. Its only goal is to disclose the connection of the first output to the control input of the second switch (see Claim 7 rejection). As such, the Seiler et al. reference fulfils its goal, since the diode (23 in Fig. 4 and 5), no matter how it is biased, connects the first output (collector of transistor 28) with the control input of the second switch (the base of 28).

Applicant further attacks the Seiler reference for not disclosing the DC converter (page 8, 3rd paragraph). In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In an instant case the DC converter is disclosed by Maier.

As to a forward biased diode, it is addressed in the Claim 7 rejection as follows: "The diode D2 in the Van Lempo et al. circuit addresses this limitation by providing connection between the low voltage power supply U2, which is analog to the voltage

converter 5 in Maier et al. circuit, and the first output (at the emitter of transistor T5 in Van Lempo et al.); the isolation diode (D2 in Fig. 4) is forward biased whenever the second switch (T1 in Fig. 4) is ON". Therefore, in the Van Lempo et al. circuit modified according to teachings of Maier, the first and the third outputs are interconnected via forward biased diode.

Conclusion

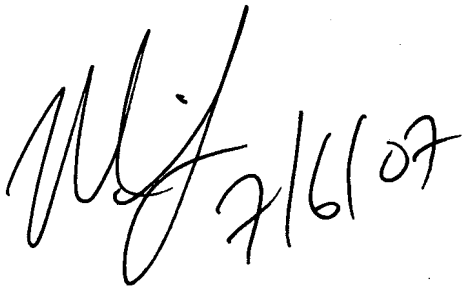
THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry,

can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
7/3/2007



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